

**PUBLIC**  
**EXHIBIT 22**

U.S. Application No. 14/614,967

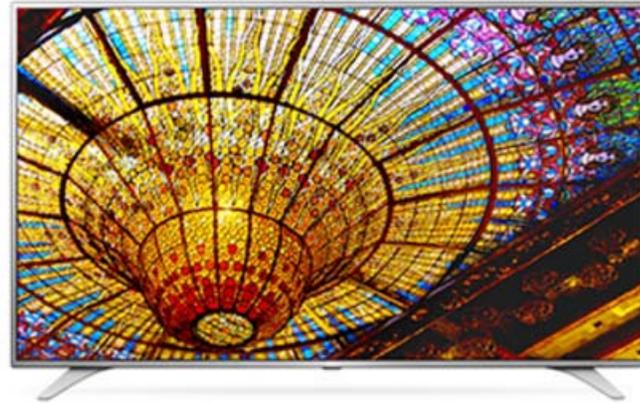
---

LG / MediaTek Products

"1. A graphics processor, comprising:"

1. A graphics processor, comprising:

The LG 49UH6500 television and X Power LS755 phone (collectively, the "LG Products") include a graphics processor.



See <http://www.lg.com/us/support-product/lg-49UH6500>.

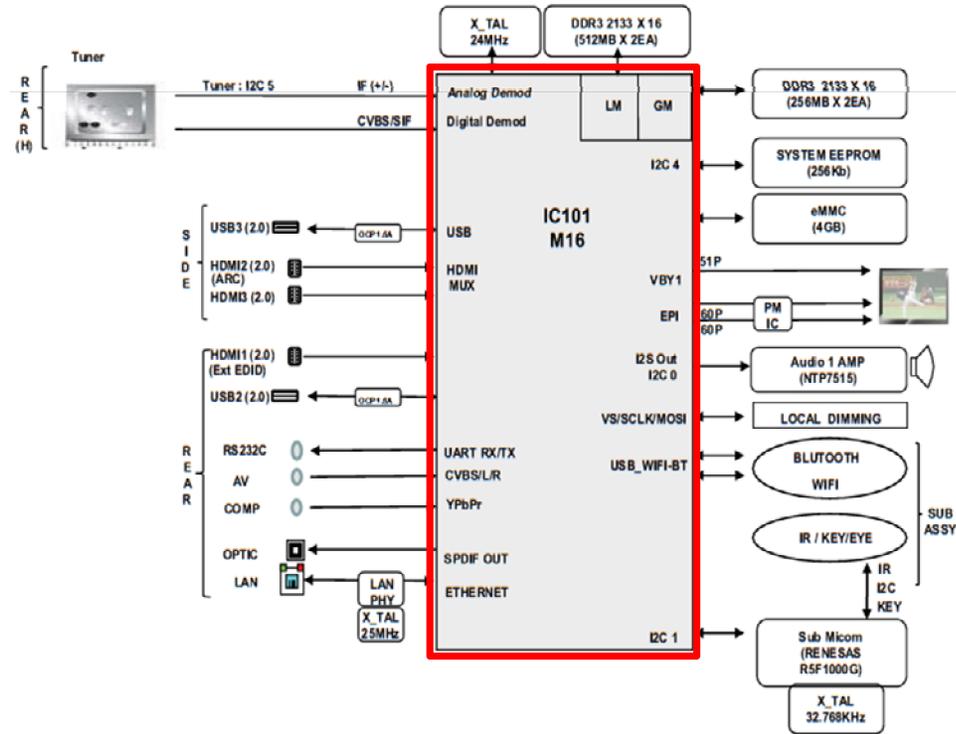
LG X power™ Boost Mobile®  
LS755  
ZOOM



See <http://www.lg.com/us/cell-phones/lg-LS755-x-power-boost-mobile>.

U.S. Application No. 14,614,967: Claim 1  
 "1. A graphics processor, comprising:"

The LG Products include one of the following System-on-Chips (SoCs): M16 and MediaTek MT6755M.



See LG LED TV Service Manual, Chassis: UA63J, Model: 43UH6500, p.28, available at [https://lg.encompass.com/shop/model\\_research\\_docs/?file=/ZEN/sm/43UH6500UB.pdf](https://lg.encompass.com/shop/model_research_docs/?file=/ZEN/sm/43UH6500UB.pdf).<sup>1/</sup>

<sup>1/</sup> The LG 49UH6500 television and the LG 43UH6500 television are part of the LG UH6500 Series televisions. See [http://www.lg.com/us/support/products/documents/UH6500\\_Series\\_Spec\\_Sheet\\_Updated\\_10112016.pdf](http://www.lg.com/us/support/products/documents/UH6500_Series_Spec_Sheet_Updated_10112016.pdf).

"1. A graphics processor, comprising:"

## Technical Specifications

Carrier	Boost Mobile®
Display	5.3" (1280 x 720) HD TFT Display
Battery	4,100 mAh non-removable
Platform	Android 6.0.1 Marshmallow
Processor	MediaTek 1.8 GHz Octa-Core MT6755M

See <http://www.lg.com/us/cell-phones/lg-LS755-x-power-boost-mobile>.

The SoCs include one of the following ARM Mali graphics processing units (the "Mali GPUs"): T760 MP2 and T860 MP2.

		M16
Smart Function	CPU	CA53 x4 1.1GHz / 1MB
	GPU	Mali T760 MP2 (650MHz)
	OSD	Separated 2K@60p
	HEVC	4K @60, 10bit
	DDR	DDR3-2133/ DDR4-2400
	Audio DSP	HiFi3 Dual @370MHz

See LG LED TV Service Manual, Chassis: UA63J, Model: 43UH6500, p.123, available at [https://lg.encompass.com/shop/model\\_research\\_docs/?file=/ZEN/sm/43UH6500UB.pdf](https://lg.encompass.com/shop/model_research_docs/?file=/ZEN/sm/43UH6500UB.pdf).

"1. A graphics processor, comprising:"

**MediaTek MT6755 Helio P10 Specs**

<b>Release</b>	Q4 2015
<b>Process</b>	28nm
<b>Apps CPU</b>	8x Cortex-A53, up to 2.0GHz
<b>GPU</b>	<b>ARM Mali-T860 MP2 at 700 MHz</b>

*See <http://cnoemphone.com/blog/mediatek-mt6755-helio-p10-specs-benchmark-and-smartphone-list>.*

The Mali GPUs share substantially similar structure, function, and operation.



### High performance

With stunning graphics capabilities, ARM Mali High Performance GPUs combine GPU Compute functionality with micro-architecture enhancements and system-wide, bandwidth-saving technology to bring energy efficiency to advanced mobile and consumer devices. GPU Compute solutions enable each task to be executed on the most suitable processor within the system. The resultant efficiencies guarantee superior graphics performance and extended battery life.

High performance GPUs:

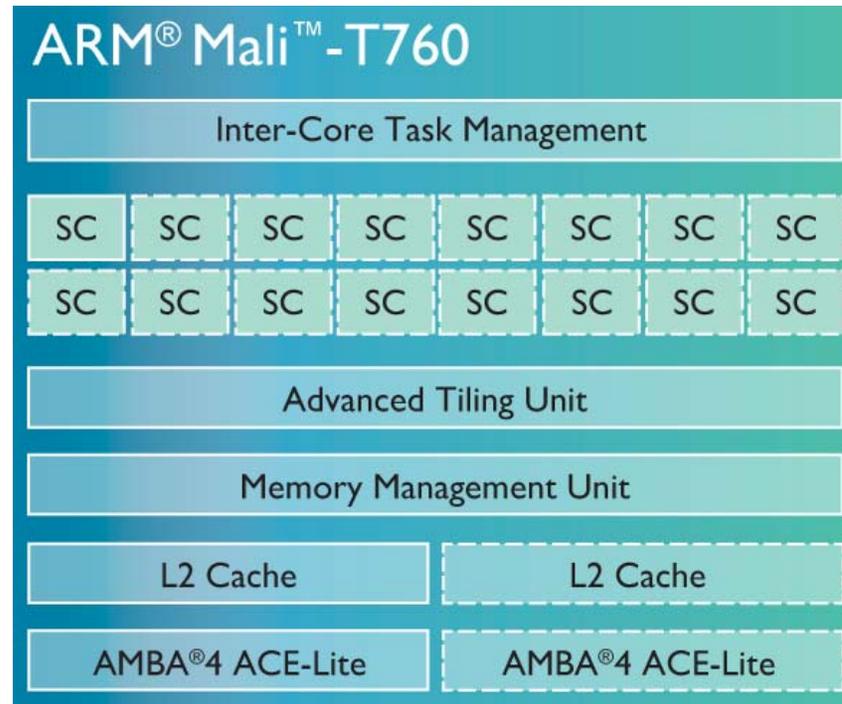
- Mali-G71
- Mali-T860 & T880
- Mali-T760
- Mali-T628
- Mali-T624

See <http://www.arm.com/products/graphics-and-multimedia/mali-gpu>.

a unified shader; and

The graphics processor in the LG Products includes a unified shader.

For example, the Mali GPUs implement the unified shader architecture.



See <http://www.arm.com/products/multimedia/mali-gpu/high-performance/mali-t860-t880.php>.

#### GPU Architecture

The "Midgard" family of Mali GPUs (the Mali-T600 and Mali-T700 series) use a unified shader core architecture, meaning that only a single type of shader core exists in the design. This single core can execute all types of programmable shader code, including vertex shaders, fragment shaders, and compute kernels.

See <https://community.arm.com/groups/arm-mali-graphics/blog/2014/03/12/the-mali-gpu-an-abstract-machine-part-3--the-shader-core>.

"an arbiter circuit operative to carry out an arbitration scheme to determine which of a plurality of inputs to provide to the unified shader;"

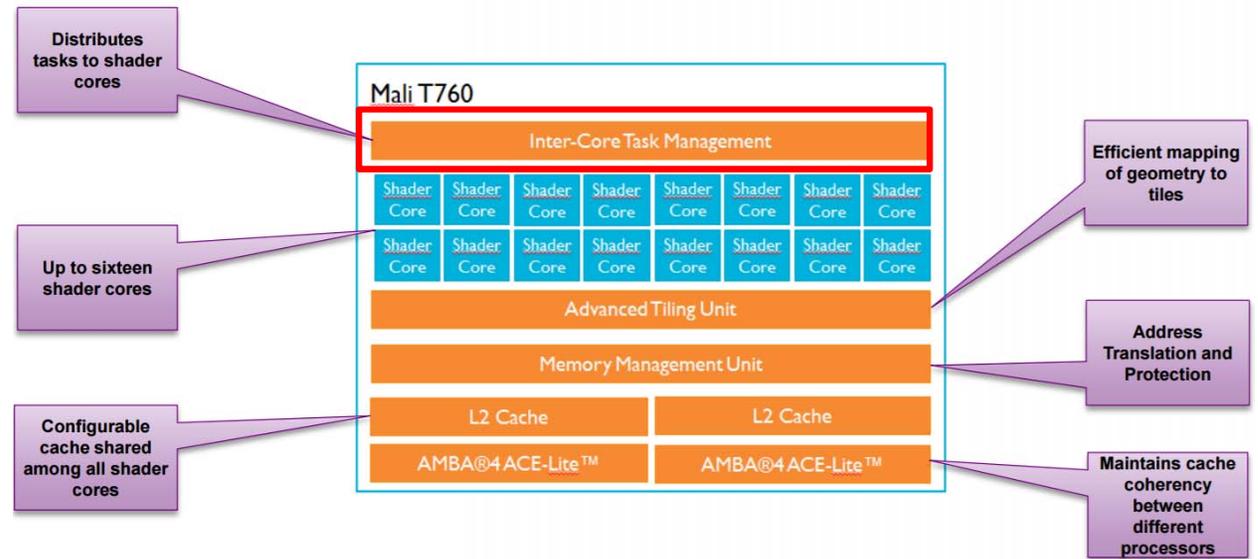
an arbiter circuit operative to carry out an arbitration scheme to determine which of a plurality of inputs to provide to the unified shader;

The LG Products include an arbiter circuit operative to carry out an arbitration scheme to determine which of a plurality of inputs to provide to the unified shader.

For example, the Mali GPUs include the Inter-Core Task Management unit.

The shared hardware in Midgard is primarily concerned with managing the interaction of the shader cores, followed by providing the L2 cache and all further memory interfaces for accessing main memory and/or the CPU cache. In the case of Mali-T760 there is **1 task management unit** and memory management unit, but 2 sets of L2 cache and the AMBA interface that connects the GPU to the rest of the system.

See <http://www.anandtech.com/show/8234/arms-mali-midgard-architecture-explored/4>.



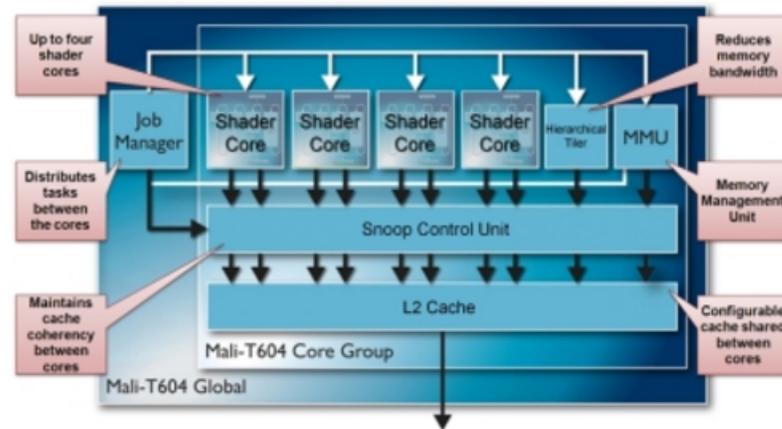
See [http://malideveloper.arm.com/downloads/ARM\\_Game\\_Developer\\_Days/PDFs/2-Mali-GPU-architecture-overview-and-tile-local-storage.pdf](http://malideveloper.arm.com/downloads/ARM_Game_Developer_Days/PDFs/2-Mali-GPU-architecture-overview-and-tile-local-storage.pdf).

The Mali GPUs are operative to carry out an arbitration scheme to determine which of a plurality of inputs to provide to the unified shader. For example, the Job Manager “can dynamically move threads among the shaders.”

"an arbiter circuit operative to carry out an arbitration scheme to determine which of a plurality of inputs to provide to the unified shader;"

Adding a bit more detail, the T604 includes four shader cores, each of which contains two arithmetic pipelines, one texturing pipeline, and one load/store unit. The four shaders share a coherent L2 cache, an MMU, a tiler, and a Job Manager. This latter block is a key component because the shaders are multithreaded. **The Job Manager can dynamically move threads among the shaders.**

### Mali-T604 high-level architecture



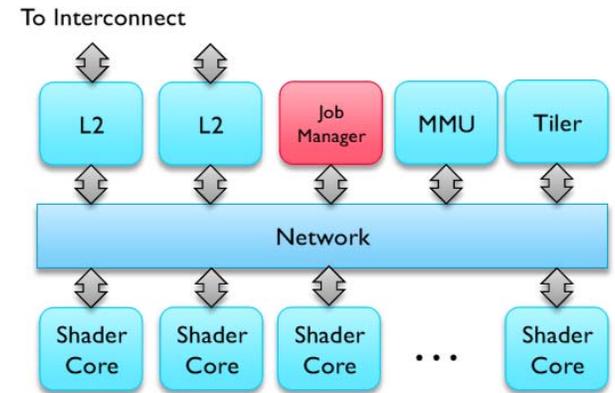
This dynamic load allocation, in turn, allows the host system to exert considerable control over the energy consumption of the core—vital to high-performance mobile use. But it also requires that the threads be light-weight. And that puts stress on the L2 cache, which must hold any state not local to the shader.

See [http://www.eetimes.com/document.asp?doc\\_id=1278897](http://www.eetimes.com/document.asp?doc_id=1278897).

"an arbiter circuit operative to carry out an arbitration scheme to determine which of a plurality of inputs to provide to the unified shader;"

## Mali-T880 GPU Block Diagram - Job Manager

- Fixed function block responsible for interfacing with the driver
  - Reads job descriptors from memory
  - Tracks inter-job dependencies
  - Distributes jobs across shader cores
  - Splits jobs into per-core tasks



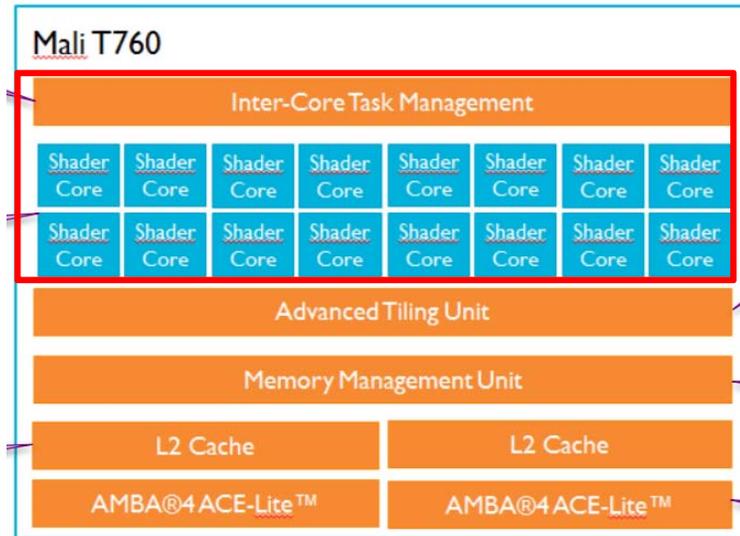
See ARM, The ARM Mali –T880 Mobile GPU, p.9, available at [http://www.hotchips.org/wp-content/uploads/hc\\_archives/hc27/HC27.25-Tuesday-Epub/HC27.25.50-GPU-Epub/HC27.25.531-Mali-T880-Bratt-ARM-2015\\_08\\_23.pdf/](http://www.hotchips.org/wp-content/uploads/hc_archives/hc27/HC27.25-Tuesday-Epub/HC27.25.50-GPU-Epub/HC27.25.531-Mali-T880-Bratt-ARM-2015_08_23.pdf/).

"wherein the unified shader is operatively coupled to the arbiter circuit and comprises:"

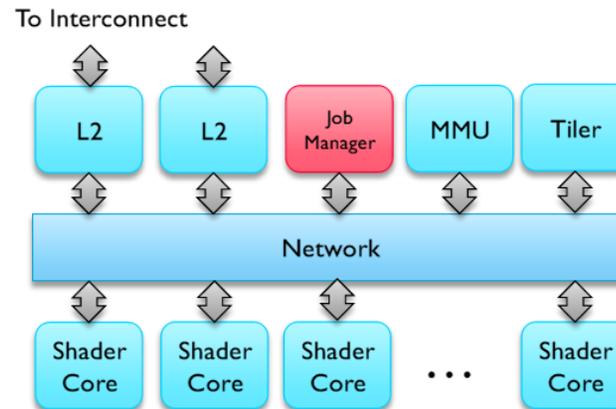
wherein the unified shader is operatively coupled to the arbiter circuit and comprises:

The unified shader is operatively coupled to the arbiter circuit.

For example, in the Mali GPUs, unified shaders (SCs) are coupled to the Job Manager, a.k.a. the Inter-Core Task Management unit.



See [http://malideveloper.arm.com/downloads/ARM\\_Game\\_Developer\\_Days/PDFs/2-Mali-GPU-architecture-overview-and-tile-local-storage.pdf](http://malideveloper.arm.com/downloads/ARM_Game_Developer_Days/PDFs/2-Mali-GPU-architecture-overview-and-tile-local-storage.pdf).



See ARM, The ARM Mali –T880 Mobile GPU, p.9, available at [http://www.hotchips.org/wp-content/uploads/hc\\_archives/hc27/HC27.25-Tuesday-Epub/HC27.25.50-GPU-Epub/HC27.25.531-Mali-T880-Bratt-ARM-2015\\_08\\_23.pdf/](http://www.hotchips.org/wp-content/uploads/hc_archives/hc27/HC27.25-Tuesday-Epub/HC27.25.50-GPU-Epub/HC27.25.531-Mali-T880-Bratt-ARM-2015_08_23.pdf/).

“a processor unit configured to simultaneously perform vertex manipulation operations and pixel manipulation operations based on the provided inputs to the unified shader.”

a processor unit configured to simultaneously perform vertex manipulation operations and pixel manipulation operations based on the provided inputs to the unified shader.

The LG Products include a processor unit configured to simultaneously perform vertex manipulation operations and pixel manipulation operations based on the provided inputs to the unified shader.

For example, the Mali GPUs include the unified shader architecture, where each shader core (SC) includes a Tri-pipe that runs multiple threads at the same time. Even if some thread is stalled waiting for memory, the Tri-pipe still runs the other threads.

**Massively Multi-threaded Machine**

Unlike a traditional CPU architecture, where you will typically only have a single thread of execution at a time on a single core, the tripipe is a massively multi-threaded processing engine. There may well be hundreds of hardware threads running at the same time in the tripipe, with one thread created for each vertex or fragment which is shaded. This large number of threads exists to hide memory latency; it doesn't matter if some threads are stalled waiting for memory, as long as at least one thread is available to execute then we maintain efficient execution.

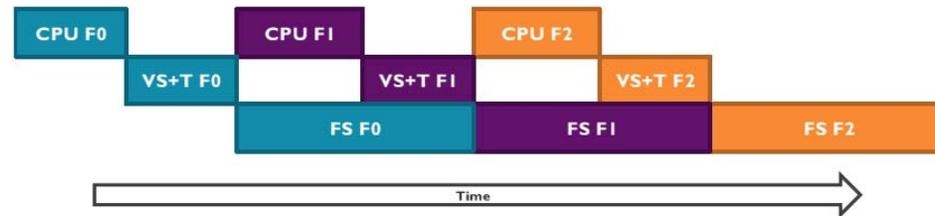
*See <https://community.arm.com/groups/arm-mali-graphics/blog/2014/03/12/the-mali-gpu-an-abstract-machine-part-3--the-shader-core>.*

The Mali GPUs are configured to simultaneously perform vertex manipulation operations and pixel manipulation operations.

“a processor unit configured to simultaneously perform vertex manipulation operations and pixel manipulation operations based on the provided inputs to the unified shader.”

## Mali-T880 Rendering Flow - Pipelining Vertex and Fragment Jobs

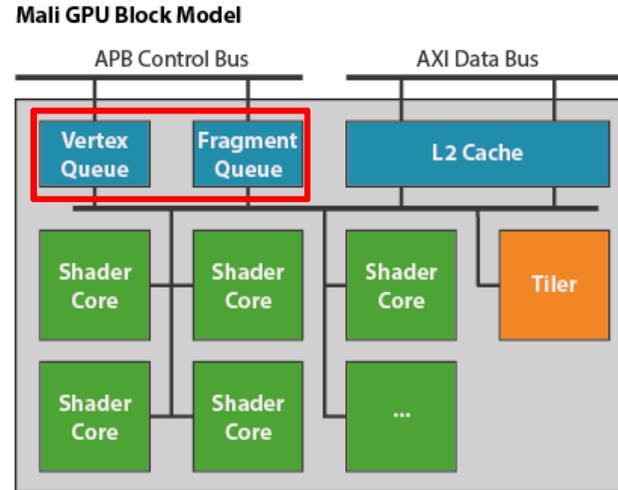
- Mali GPU functionality is configured using descriptors
  - Memory-resident data structures
  - Control most aspects of GPU functionality
  - Very little is controlled via registers
- Mali GPUs support simultaneous vertex and fragment shading
- Vertex and Tiling jobs are sent to the GPU as a single job
- Rendering is pipelined
  - Vertex shading for RT N+1 running at the same time as fragment shading for RT N



See ARM, The ARM Mali –T880 Mobile GPU, p.9, available at [http://www.hotchips.org/wp-content/uploads/hc\\_archives/hc27/HC27.25-Tuesday-Epub/HC27.25.50-GPU-Epub/HC27.25.531-Mali-T880-Bratt-ARM-2015\\_08\\_23.pdf/](http://www.hotchips.org/wp-content/uploads/hc_archives/hc27/HC27.25-Tuesday-Epub/HC27.25.50-GPU-Epub/HC27.25.531-Mali-T880-Bratt-ARM-2015_08_23.pdf/).

In addition, the Mali GPUs perform the vertex manipulation operations and pixel manipulation operations based on the provided inputs to the unified shader. For example, the Mali GPU performs pixel and vertex manipulation operations based on the inputs provided by a Vertex Queue, Fragment Queue, Fragment Thread Creator, Vertex Thread Creator, Thread Pool, and/or Thread Issue.

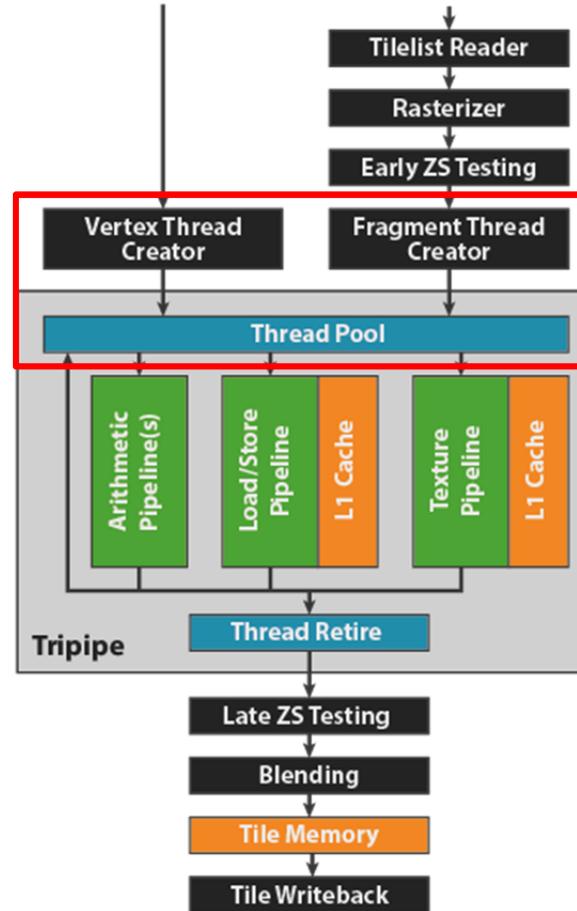
“a processor unit configured to simultaneously perform vertex manipulation operations and pixel manipulation operations based on the provided inputs to the unified shader.”



See The Mali GPU: An Abstract Machine, Part 3 - The Midgard Shader Core, <https://community.arm.com/groups/arm-mali-graphics/blog/2014/03/12/the-mali-gpu-an-abstract-machine-part-3--the-shader-core>.

“a processor unit configured to simultaneously perform vertex manipulation operations and pixel manipulation operations based on the provided inputs to the unified shader.”

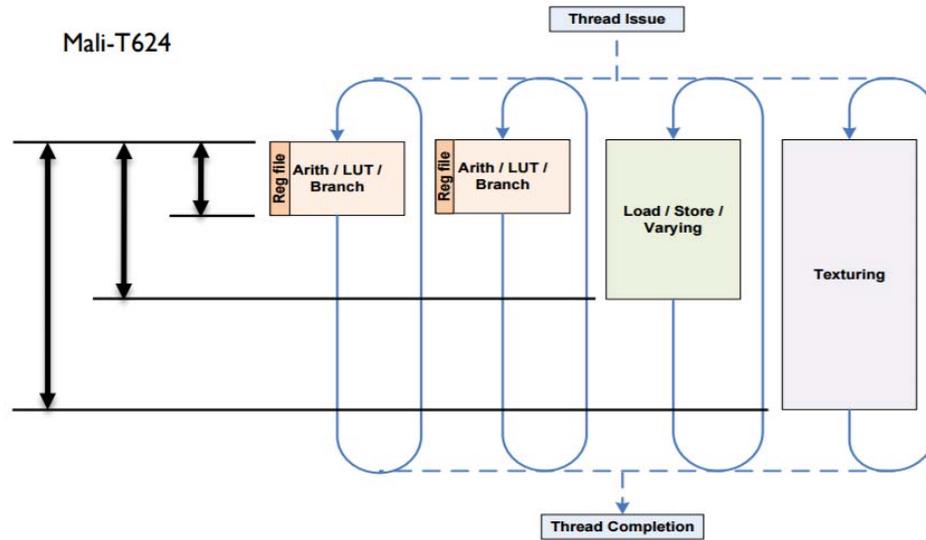
**Mali Shader Core Block Model**



See The Mali GPU: An Abstract Machine, Part 3 - The Midgard Shader Core, <https://community.arm.com/groups/arm-mali-graphics/blog/2014/03/12/the-mali-gpu-an-abstract-machine-part-3--the-shader-core>.

“a processor unit configured to simultaneously perform vertex manipulation operations and pixel manipulation operations based on the provided inputs to the unified shader.”

## Tri-pipe Architecture



- Unified shader architecture
  - Fragment and vertex shaders
  - Geometry and compute shaders
- Very high throughput graphics
- Multiple parallel pipelines
  - Two low-latency arithmetic pipes
  - 256 simultaneous threads
  - Low-latency for computation

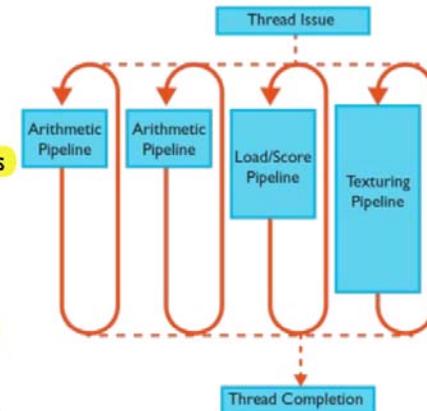
See [http://malideveloper.arm.com/downloads/ARM\\_Game\\_Developer\\_Days/PDFs/2-Mali-GPU-architecture-overview-and-tile-local-storage.pdf](http://malideveloper.arm.com/downloads/ARM_Game_Developer_Days/PDFs/2-Mali-GPU-architecture-overview-and-tile-local-storage.pdf).

“a processor unit configured to simultaneously perform vertex manipulation operations and pixel manipulation operations based on the provided inputs to the unified shader.”

## ARM® Mali™-T628 GPU Tripipe

### Tripipe Cycles

- Arithmetic instructions
  - Math in the shaders
- Load & Store instructions
  - Uniforms, attributes and varyings
- Texture instructions
  - Texture sampling and filtering
- Instructions can run in parallel
  - Each one can be a bottleneck
  - There are two arithmetic pipelines so we should aim to increase the arithmetic workload



See ARM, ARM Tools Part 2, Best Optimization Practices for Mobile Platforms, p.11, available at [http://malideveloper.arm.com/downloads/ARM\\_Game\\_Developer\\_Days/PDFs/6%20-%20ARM%20Tools%20Part%202-%20Best%20Optimization%20Practices%20for%20Mobile%20Platforms.pdf](http://malideveloper.arm.com/downloads/ARM_Game_Developer_Days/PDFs/6%20-%20ARM%20Tools%20Part%202-%20Best%20Optimization%20Practices%20for%20Mobile%20Platforms.pdf).